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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, December 2015
(2008 Scheme)
08.305 : DIGITAL SYSTEM DESIGN (R, F)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions :

1. Perform the following number conversions
   a) $(163.6)_{10}$ to binary
   b) $(ABC.1F)_{16}$ to octal
   c) $(10101.11)_2$ to decimal
   d) $(141.5)_{10}$ to Hexa decimal

2. What do you mean by self complementing code ? Give one example. What is the condition for a weighted code to be self complementing ?
3. Using 15's compliment perform :
   a) ABC5.61 – 937F.AB
   b) 3FC.73 – ABC.9F.
4. Define hamming distance. What do you mean by cyclic code ? Give one example.
5. What are the steps to be followed to realize a function in the form of sum of products using only NAND gates ?
6. Give the most simplified form of the function f = Σ 1, 2, 6, 9, 13, 14, 15 using K-map.

P.T.O.

7. Implement the following function using only NOR gates :

   $f = \bar{a}bc + abc + a\bar{b} + d$.

8. Give the excitation tables of SR flip-flop and T-Flip-flop.

9. Differentiate between synchronous and asynchronous sequential circuits.

10. Draw the circuit of a Johnson counter using 4-D flip-flops and show the sequence of states it will go through starting from 0000. **(10×4=40 Marks)**

PART – B

Answer **one** question from **each** Module :

Module – I

11. a) Perform the following operations using 8421 code : **10**

    i) 169.73 + 113.69

    ii) 693.67 – 373.60 using 9's complement.

    b) Perform the following operations using excess-3 code : **10**

    i) 169.73 + 113.69

    ii) 693.67 – 373.60 using 9's complement.

OR

12. a) Perform the following : **12**

    i) 38FB + 2FCD

    ii) $(383.63)_{10} - (493.73)_{10}$ using 10's complement

    iii) $(373.61)_8 - (107.73)_8$ using 7's complement

    iv) $(101101.11)_2 - (111011.101)_2$ using 1's complement.

    b) Illustrate the representation of floating point numbers. Explain various steps involved in adding two floating point numbers. **8**

Module – II

13. a) Design a full adder circuit using only NAND gates. Show that a full adder can be designed using two half adders. **10**

    b) Simplify the following expressions using K-map. **10**

    i) $f = \Sigma\ 0, 1, 2, 7, 9, 10, 13, 14.$

    Get the simplified expression in sum of product form

    ii) $z = \Sigma\ 1, 2, 7, 9, 11, 12, 15$ get the simplified expression in product of sum form.

OR

14. a) Design a logic circuit for converting excess-3 code to 8421 code. **12**

    Draw the circuit using only NAND.

    b) Using a 4×1 multiplexer is realize the function

    $f = \Sigma 0, 1, 5, 6, 7.$ **8**

Module – III

15. Design a modulo – 10 synchronous counter using J-K flip-flop. Draw the circuit using JK flip-flops and suitable gates. Also give the excitation table of JK flip flop. **20**

OR

16. a) Explain the working of edge triggered JK flip-flops using NAND gates. **15**

    b) Show how a JK flip-flop is converted to D-flip-flop and T-flip-flop. **5**
